Closed-loop DC-link Voltage Balancing Algorithm for a Four-level π-type Converter

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***Abstract*—A four-level π-type converter is a Neutral Point Clamped (NPC) multilevel converter topology for low/medium voltage applications. As the inherent issue with this topology, the DC-link capacitor voltage balancing is challenging, especially when it operates as a single-end inverter/rectifier with unity power factor. This paper proposes a closed-loop DC-link voltage balancing algorithm of a π-type converter that is effective and simple to implement. In principle, this approach is based on Redundant Level Modulation (RLM). The RLM utilizes additional voltage levels in each switching window to gain extra controllability of the DC-link capacitor voltages without affecting the average output voltage. An algorithm based on mathematical and logical operations is developed to utilize RLM to achieve the closed-loop voltage balancing. The proposed control method is effective over the full modulation index (M = 0 ~ 1.15) and full power factor range ($\cos\varphi$ = 0 ~ 1). The algorithm is implemented in a test rig, and the experiment confirms its effectiveness.**

Keywords—multilevel converter, voltage balancing, level-shifted carrier, π-type

I. Introduction

Multilevel converters have been studied and implemented as alternative topologies for low/medium voltage, high-power applications. Compared to a conventional two-level converter, the benefits of multilevel topologies include lower *dV/dt*, lower output harmonics and lower switching loss. As an available candidate of the multilevel converter topologies, the π-type topology was proposed and has been actively researched over the past years [1]–[4]. The π-type topology is essentially a four-level converter in the Neutral-Point Clamped (NPC) family with reduced device count (six devices per phase leg). The π-type topology is illustrated in Fig. 1.

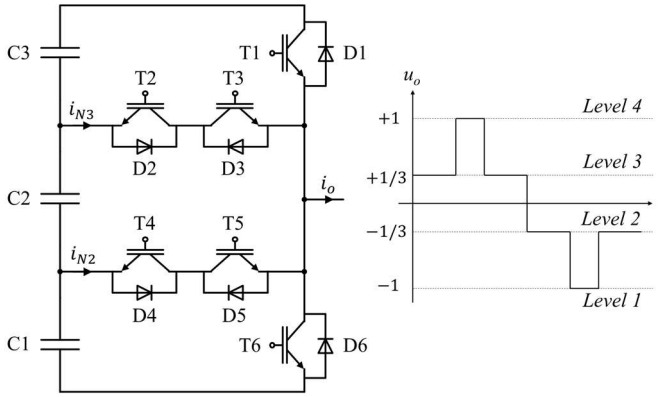

Fig. 1. Concept of a π-type converter topology with IGBTs in the common-collector configuration

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A. Capacitor voltage balancing problem in a π-type converter

The main challenge in a π-type converter is to maintain the middle capacitor voltage, especially under unity power factor [1]–[3]. In order to operate normally, the three DC-link capacitors voltages must maintain at 1/3 of the whole DC-link voltage. As analyzed in [1], when the load current is positive, outputting the voltage *level 3* leads to the discharge of the capacitor C2. When the load current is negative, outputting the voltage *level 2* also leads to the discharge of the capacitor C2. Subsequently, the converter operate at unity power factor leads to only the discharge of capacitor C2 as illustrated in Fig. 2. If the middle capacitor voltage is balanced, the two outer capacitor voltages can be naturally balanced over a fundamental cycle as analyzed in [5].

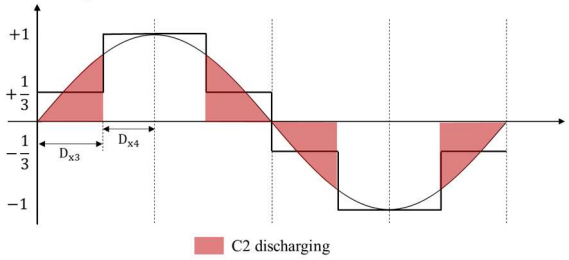

Fig. 2. Charge/discharge status of C2 with ordinary modulation ($\cos\varphi$ = 1)

B. Limitations of the existing voltage-balancing methods

To achieve the voltage balancing of a four-level NPC converter, numerous research efforts have been made previously (e.g. [1]–[3], [5]–[9]). Generally, one approach to balance the capacitor voltages in multilevel converters is utilizing the redundant switching states within a phase leg (e.g.[10]). However, in a four-level NPC converter, there is no redundant switching states.

As another widely used approach, Zero-sequence Signal Injection (ZSI) is one degree of freedom to achieve the voltage balancing control [1]–[3], [11]. This approach is essentially equivalent to the Space Vector Modulation (SVM) presented in [12], which alters the three-phase reference voltages without affecting the line-to-line output voltages. As an representative case, [1] presents the voltage balancing control of a π-type converter based on ZSI. However, due to the limitations of ZSI, this approach is only fully effective in a back-to-back configuration in which the control challenge is moderated as a result of having two active ends. When there is only a single end (as an inverter or a rectifier), this approach cannot maintain effective at high power factor and high modulation index [1].

As the third degree of freedom, utilizing redundant output voltage levels within one switching window has been exploited in recent studies for the voltage balancing of various topologies, e.g. [6], [13], [14]. Following this principle, [5] proposed an special modulation technique to achieve the voltage balancing of the middle capacitor in a 4-level NPC converter. The approach in [5] results in utilizing three available output voltage levels in each switching window instead of two levels, for the purpose of voltage balancing. The authors stated that the control method is effective over the full modulation index, with a case of M = 0.9 confirmed in the experiment. But it is not clear whether this method still works in the expended modulation range, i.e. 1≤ M ≤ 1.15. Moreover, this proposed approach is essentially an open-loop control that maintains equal charge/discharge of the middle capacitor C2 within each switching cycle. Theoretically, if there is an initial unbalance of the capacitor voltages, this method cannot pull back the unbalance due to its open-loop nature. Studies [6]–[9] are also base on utilizing the redundant output voltage levels for the voltage balancing. However, the authors in [6] claimed their proposed control scheme are limited up to $M \approx 1.10$ with $M \approx 1.05$ confirmed in the experiment. Additionally, the approach in [6]–[9] involves complex compensator parameters and modulators that are challenging to establish from scratch and are difficult to be transferred between setups.

This work proposes a closed-loop voltage-balancing control for a π-type converter that is simple to implement with carrier-based modulation and effective over full operation conditions. The principles and the implementation of the proposed approach are elaborated in the following sections. Experiments are conducted to verify the effectiveness of the approach.

II. Proposed Closed-Loop Voltage Balancing Control

A. Principles

This paper proposes an approach that utilizes the redundant output voltage levels to gain the controllability of the middle DC-link capacitor voltage, which is referred as Redundant Level Modulation (RLM) in this work. In a π-type converter, by introducing an additional voltage level (the redundant level), the charging/discharging status of the middle capacitor can be manipulated. As illustrated in Fig. 3, the existence of the *level 2* in the first switching window leads to a charging duration for the middle capacitor that does not exist in Fig. 2, while the average output voltage of this window is unaffected. The use of *level 2* is redundant for synthesising the output voltage, but it can lead to the manipulation of the middle capacitor voltage.

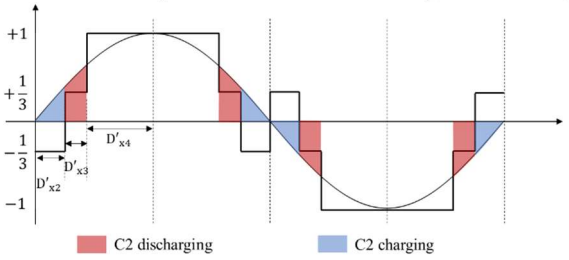

Fig. 3. Charge/discharge status of the middle capacitor C2 with redundant output voltage level introduced (power factor = 1)

The deviation of the middle capacitor voltage is defined as

$$\Delta U_{C2} = U_{C2-ref} - U_{C2} \tag{1}$$

The reference value of middle capacitor voltage $U_{C2\text{-ref}}$ is normally the 1/3 of the total DC-link voltage, but it can also be given as an individual command.

To pull the ΔU_{C2} back to zero within one switching window, the desired average neutral point currents (reference direction defined in Fig. 1) need to satisfy the following equation [5]

$$\Delta U_{C2} = \frac{1}{3} \cdot \frac{\bar{i}_{N2-ref} - \bar{i}_{N3-ref}}{C \cdot f_{sw}} \tag{2}$$

Subsequently, the middle capacitor voltage can be controlled by controlling the difference of these two neutral point currents ($i_{N2} - i_{N3}$). In each switching cycle, the average neutral point currents are contributed by three-phase load currents as

$$\bar{i}_{N2} = I_a D_{a2} + I_b D_{b2} + I_c D_{c2} \tag{3}$$

$$\bar{i}_{N3} = I_a D_{a3} + I_b D_{b3} + I_c D_{c3} \tag{4}$$

Where I_x is the phase load current; D_{x2}/D_{x3} are the duty ratios of the output voltage *level 2* or *level 3*. Therefore, the control of the neutral point currents can be achieved by manipulating the D_{x3} and D_{x2} of all phases ($x = a, b, c$). Similar to [11], [15], the manipulation of D_{x3} and D_{x2} is independent between the three phases. To obtain the control objective for one individual phase, a simplified phase command is used in this approach as

$$I_x(D_{x2-ref} - D_{x3-ref}) = (\bar{i}_{N2-ref} - \bar{i}_{N3-ref})/3 = A \tag{5}$$

To find the appropriate alteration of D_{x3} and D_{x2}, the following example is given when the reference voltage $U_{x\text{-ref}}$ is positive. In this case, *level 4, level 3* and *level 2* are utilized as shown in Fig. 3. Firstly, the following equation must be satisfied for the three duty ratios

$$D_{x4-ref} + D_{x3-ref} + D_{x2-ref} = 1 \tag{6}$$

To satisfy the reference output voltage, the following equation must stand

$$D_{x4-ref} + \frac{1}{3} D_{x3-ref} - \frac{1}{3} D_{x2-ref} = U_{x-ref} \tag{7}$$

Equation (5)-(7) contains three variable that are solvable. The solved reference value $D_{x3\text{-ref}}$ is

$$D_{x3-ref} = -(4A - 3I_x + 3I_x U_x)/6I_x \tag{8}$$

However, the control command A can be unreasonable depending on the degree of imbalance. In principle, this command always attempts to pull back the imbalance within one switching cycle no matter how large the imbalance is. Therefore, the solved duty ratios must be trimmed by applying an upper/lower limit. Comparing Fig. 2 and Fig. 3, it can be seen that, when the reference voltage is positive, the main degree of freedom is to shrink D_{x3} and introduce additional D_{x4} and D_{x2} to maintain the same output volt-time product. In this case, the trim is done on the D_{x3}. There are two constraints that limits the modified duty ratio D'_{x3}. Constraint (9) ensures the

modified D'_{x3} to be equal to/smaller than the original value D_{x3}. By setting up this rule along with (7), it is ensured that the converter output voltage and the maximum modulation index is not undermined.

$$D'_{x3} \leq D_{x3} \tag{9}$$

Constraint (10) ensures that there is a "dwell time" [14] to maintain the operation as a multilevel converter with reduced *dV/dt*. This dwell time is determined as a pre-defined deadtime in this work.

$$D'_{x3} \cdot T_{sw} \geq T_{deadtime} \tag{10}$$

If the reference value $D_{x3\text{-ref}}$ is beyond these two boundaries, it will be limited in order to produce a reasonable D'_{x3}. Once the trimmed D'_{x3} is derived, the other two modified duty ratios D'_{x4} and D'_{x2} can be calculated by solving (6) and (7) as

$$D'_{x4} = \frac{3}{4}U_x - \frac{1}{2}D'_{x3} + \frac{1}{4} \tag{11}$$

$$D'_{x2} = -\frac{3}{4}U_x - \frac{1}{2}D'_{x3} + \frac{3}{4} \tag{12}$$

This whole process of finding and applying the modified D'_{x3} leads the power converter to operate towards the control objective *A*, which result in the precise control of the middle capacitor voltage U_{c2}. This process is conducted for all three phases individually. Additionally, when the reference voltage U_x is negative, *level 3, level 2* and *level 1* are used instead as shown in Fig. 3, with the trim performed on D'_{x2}.

B. Implementation with level-shifted carriers

The proposed RLM approach can be implemented through various modulation techniques. In multilevel converters, the most commonly used modulation scheme is the level-shifted carrier PWM for simple implementation, such as [1]. Based on the level-shifted carrier PWM, the RLM operation can be achieved by split and modify the modulating waves as in [11], [16], although this approach was only implemented for three-level NPC converters in these previous studies.

In this approach, the modulating wave is split to three signals that correspond to the three level-shifted carriers. Fig. 4 shows a zoomed-in switching cycle to demonstrate how the RLM operation is realized by altering the split modulating waves.

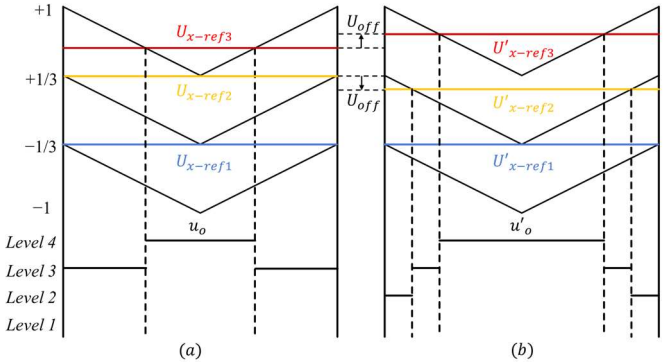

Fig. 4. Illustration of the level-shifted carriers and modulating waves in one switching window ($U_{x\text{-ref}} > 0$) (a) SPWM with split modulating waves (b) proposed RLM with level-shifted carriers

Because the switching frequency f_{sw} is much higher than the fundamental frequency f_0, the reference voltages can be considered constant in this view. By injecting an offset voltage U_{off} through (13), the phase output voltage u_o is changed from Fig. 4(a) to Fig. 4(b).

$$\begin{cases} U'_{x-ref3} = U_{x-ref3} + U_{off} \\ U'_{x-ref2} = U_{x-ref2} - U_{off} \end{cases}, (U_{x-ref} > 0)$$
$$\begin{cases} U'_{x-ref2} = U_{x-ref2} + U_{off} \\ U'_{x-ref1} = U_{x-ref1} - U_{off} \end{cases}, (U_{x-ref} \leq 0) \tag{13}$$

In Fig. 4(b), the redundant voltage level is achieved without affecting the average output voltage of this window. Following the geometrical relationships, the offset voltage $U_{off} \geq 0$ can be calculated from the desired duty ratios as

$$U_{off} = \begin{cases} (D_{x3} - D'_{x3-ref})/3, & x > 0 \\ (D_{x2} - D'_{x2-ref})/3, & x \leq 0 \end{cases} \tag{14}$$

Fig. 5 shows a zoomed-out view of a fundamental cycle of the original modulating wave, the split modulating waves and the altered modulating waves.

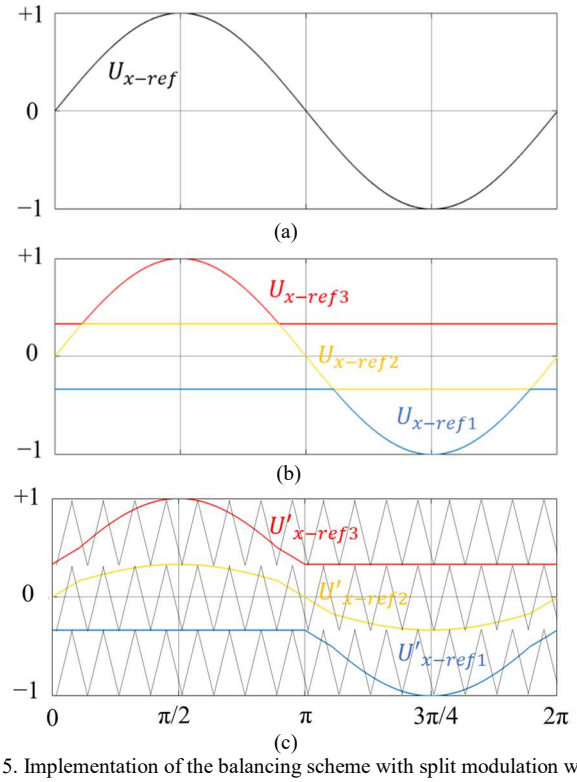

Fig. 5. Implementation of the balancing scheme with split modulation wave method ($M = 1$, $A = 0$) (a) original sinusoidal wave (b) split waves (c) altered split waves for voltage balancing with three level-shifted carriers

Therefore, a process of achieving the voltage balancing can be realized through the derived mathematical equations and logical operations. Fig. 6 illustrates the flow of the proposed voltage balancing scheme. The first modification to the modulating waves is the injection of a zero-sequence signal, normally a third-order harmonic, to expand the modulation index. Secondly, depending on the polarity of the modulating wave,

there are two cases to proceed. When $U_{x\text{-}ref}$ is positive, the control focus is on the D'_{x3}. When $U_{x\text{-}ref}$ is negative, the control focus is on the D'_{x2}.

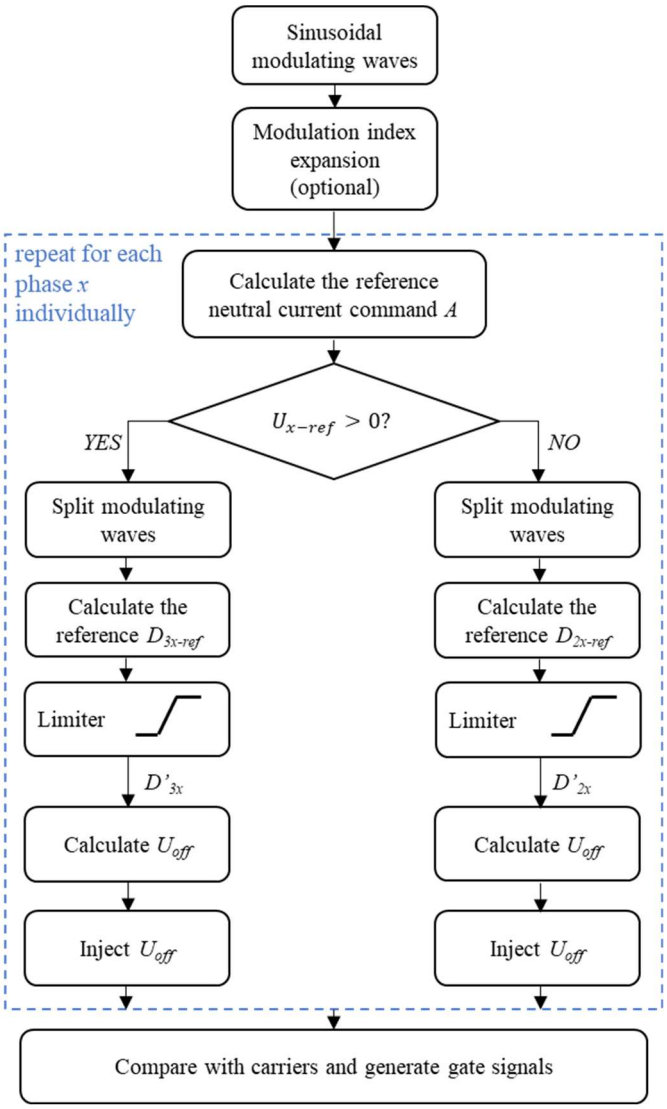

Fig. 6. Block diagram of the proposed RLM voltage balancing scheme and implementation with level-shifted carriers

Note the optional expansion of maximum modulation index (from M = 1 to 1.15) can be achieved through injecting the following zero-sequence signal to the three-phase reference voltages [11], [15].

$$U_{zero} = -\frac{1}{2}\left[\max\left(U_{a-r}\ ,U_{b-ref},U_{c-ref}\right) + \min(U_{a-ref},U_{b-ref},U_{c-ref})\right] \quad (15)$$

At the end of the whole process, the gate signals are generated to reflect the altered operation on the converter. This algorithm achieves the closed-loop control of the middle capacitor voltage.

C. Merits/drawbacks of the proposed scheme

The proposed approach can be easily implemented in a Digital Signal Processor (DSP) based control system. As introduced, level-shifted-carrier based modulators are very common in multilevel converters. The proposed approach does not require any changes on the modulator end because it only manipulate the modulating waves. Moreover, the proposed approach only involves mathematical and logical operations without the use of any PI/PID controllers. This feature simplifies the implementation and the tuning process of control parameters. Additionally, the proposed approach offers a precise control towards the control objective. Instead of a fixed dwell time (see [14]), the D'_{x3} and D'_{x2} in this approach is adjusted following the control command steplessly.

From the performance point of view, this approach has been verified in simulation models built in Matlab/Simulink. The models confirm that this approach is effective in balancing the middle capacitor voltage over the full range of power factor ($\cos\varphi = 0 \sim 1$) and modulation index ($M = 0 \sim 1.15$).

Meanwhile, there are side effects of this approach while it balances the capacitor voltages. As shown in Fig. 3, introducing the redundant voltage level leads to additional switching transitions and associated switching losses. In [13], the RLM is implemented in a three-level T-type converter and the analysis shows that the switching losses can increase significantly due to the additional switching transitions. But, the increase of switching loss can be moderated by applying a lower switching frequency or applying Wide Bandgap (WBG) power devices with ultra-low switching losses.

III. Experimental Evaluation

A proof-of-concept test rig is built to validate the proposed voltage balancing scheme. The specifications of the test rig are shown in Table 1. The switching frequency is set at 5 kHz, which is a typical value for 1200 V rated IGBTs.

TABLE 1 SPECIFICATIONS OF THE TEST RIG

Fundamental frequency f_0	50 Hz
Switching frequency f_{sw}	5 kHz
DC-link voltage U_{dc}	120 V
R	22 Ω *per phase*
L	6.34 *mH per phase*

A picture of the test rig is presented in Fig. 7. The control algorithm is implemented in a DSP, TMS320F28335.

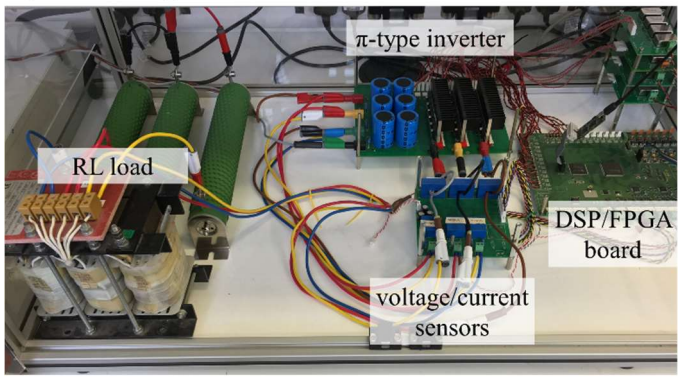

Fig. 7. Picture of the test rig

Operating at a power factor close to unity, the converter outputs a phase voltage U_a and load current I_a, which are captured and shown in Fig. 8 and Fig. 9. It can be seen that the middle capacitor voltage U_{c2} is well maintained at 40 V in two cases with full modulation index (M = 1 or 1.15) instead of getting fully discharged. For the modulation index between 0 ~ 1, the effectiveness of the proposed scheme is also confirmed for various M with a step of 0.1.

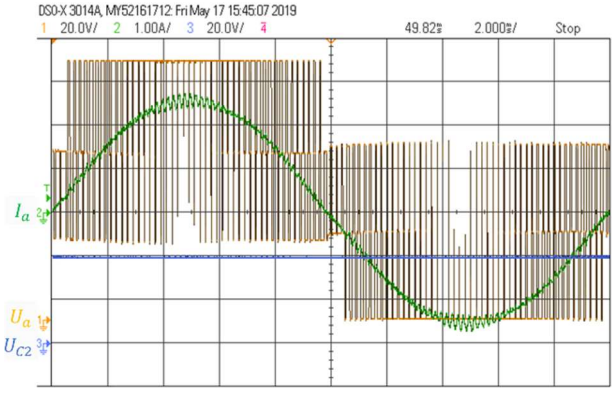

Fig. 8. Phase output voltage/current and middle capacitor voltage with M = 1

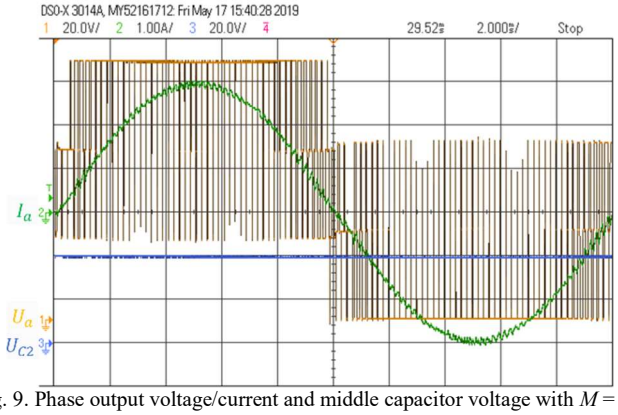

Fig. 9. Phase output voltage/current and middle capacitor voltage with M = 1.15

Fig. 10 shows a zoomed-in view of the converter behavior under the proposed voltage balancing scheme. It can be seen that the power converter outputs three voltage levels in one switching window as intended, instead of two voltage levels.

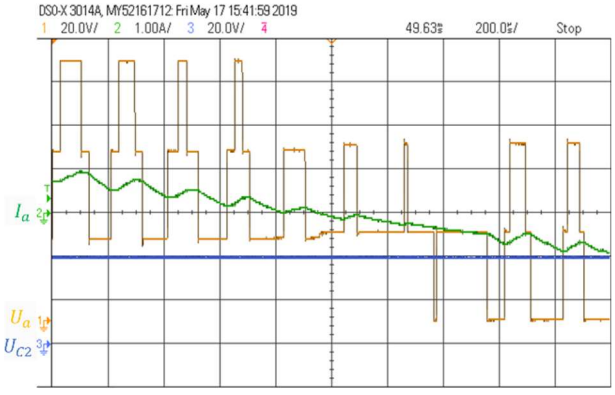

Fig. 10. Zoomed-in view of the converter behavior (M = 1.15)

Fig. 10 also shows that the outer two capacitor voltages U_{c3} and U_{c1} are naturally balanced at 1/3 of the DC-link voltage, which are reflected as the output voltages *level 2* at 40 V and *level 3* at 80 V.

Fig. 11 shows the closed-loop response of the system when a command is given to U_{c2} to change from 60 V to 40 V with a modulation index of one. The U_{c2} well follows the command and maintains at 40 V after several fundamental cycles, with the outer two capacitors balanced naturally.

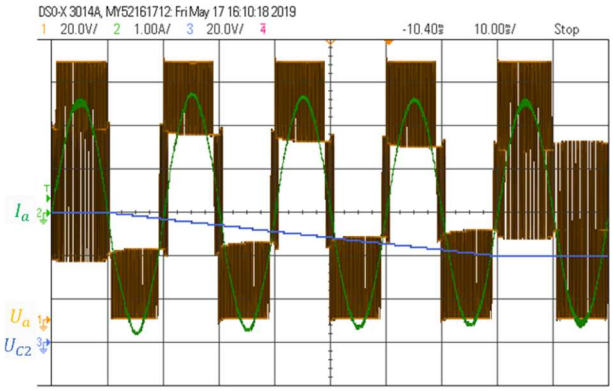

Fig. 11. Response of middle the capacitor voltage U_{C2} with a control command from 60V to 40V (M = 1)

Fig. 12 shows the three capacitor voltages in the transition where U_{c2} is controlled from 60 V to 40 V, in which the three voltages eventually settle at 1/3 of DC-link voltage.

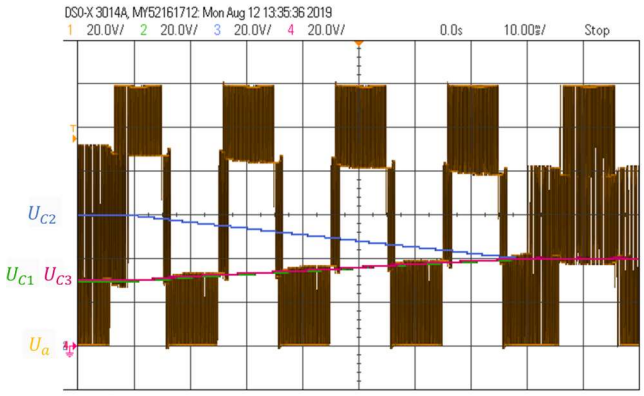

Fig. 12. Transitional capacitor voltages U_{C3}/U_{C2}/U_{C1} with a control command of U_{C2} from 60V to 40V (M = 1)

In summary, the experiments show that the proposed control algorithm works well at the worst case (M = *1 or 1.15* and unity power factor). This control scheme enables the π-type topology to be used as a single-end inverter/rectifier.

IV. Conclusion

This paper proposes a closed-loop voltage balancing algorithm for a π-type converter. The proposed approach bases on Redundant Level Modulation (RLM) that introduces additional switching transitions and voltage levels for the purpose of voltage balancing. An algorithm is proposed based on mathematical and logical operations to convert the capacitor voltage command to precise duty ratios without involving PI/PID controllers. The algorithm is implemented through split modulating waves and level-shifted carriers that can be easily

realized in DSPs. The closed-loop nature of the approach also allows the balancing of any initial imbalance. The main drawback of this approach is the additional switching transitions and associated increase of switching losses.

Experiments are conducted on a test rig, which confirms the effectiveness of the proposed voltage balancing scheme. The test rig proves that the proposed approach works well at the worst case, which is the full modulation index and unity power factor (*M = 1 or 1.15* and unity power factor). The proposed control algorithm enables the π-type topology to be used as a single-end inverter/rectifier. This approach can also be applied on other four-level NPC topology variations.

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